Suzhou Talent Microwave,Inc
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W-Band X8 MMIC Multiplier

X8/68-116GHz/14.5dBm Output Power

Model: TLRDX-2505

TLRDX-2505 is a W-band broadband octuplexerr chip which operates from 68GHz to 116GHz.When the input power is 0dBm to +4dBm, the typical value of the in-band output power is 14.5dBm, and the typical value of the adjacent sub-harmonic suppression is 12dBc.

Features:

- Output Frequency Range: 68-116GHz
- Input Power: 0~+4dBm
- Output Power: 14.5dBm Typ
- Harmonics: -12dBc
- Chip area: 3.5mmx1.3mm

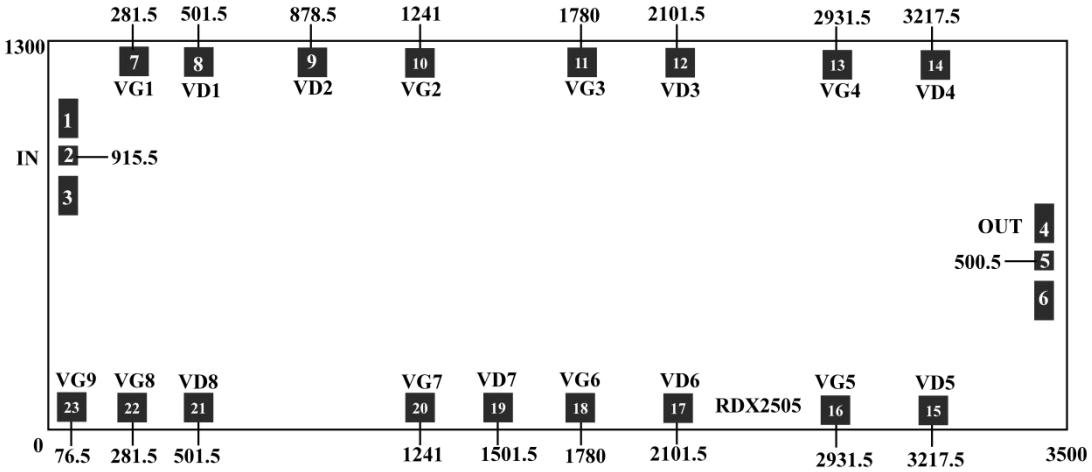
Electrical Characteristics:

Parameter	Min	Typ	Max	Units
Output Frequency	68		116	GHz
Output Power	13.3	14.5	15.2	dBm
Power Flatness@Pin=0dBm		2.1		dB
Input Frequency	8.5		14.5	GHz
Input Power	0		4	dBm
Multiply Factor		8		
Harmonics Suppression	12			dBc
Input Return Loss			-9.5	dB
Output Return Loss			-15	dB
DC Power Consumption		1030		mW

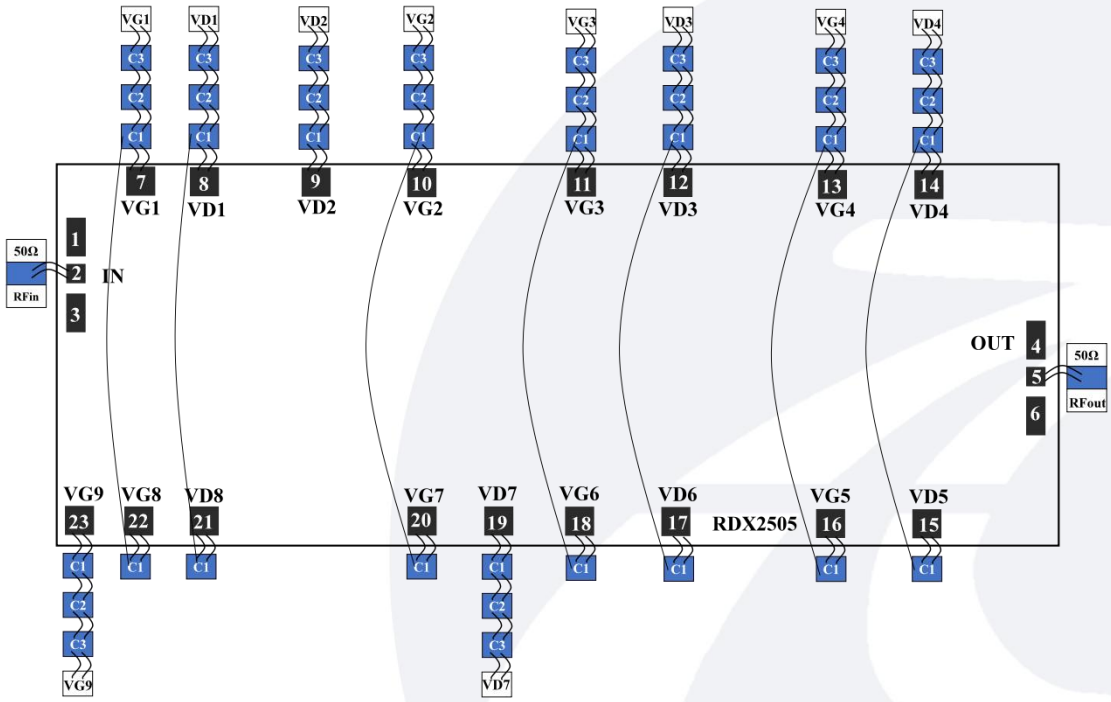
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Outline and Port size:

Unit: μm



Suggested Assembly Drawing:



Notes:

The capacitance value of peripheral capacitance C1 is 100 PF. C2 is 10000pF and C3 is 10uF. C1 it is recommended to use a single-layer capacitor and try to be close to the bonding point of the chip.

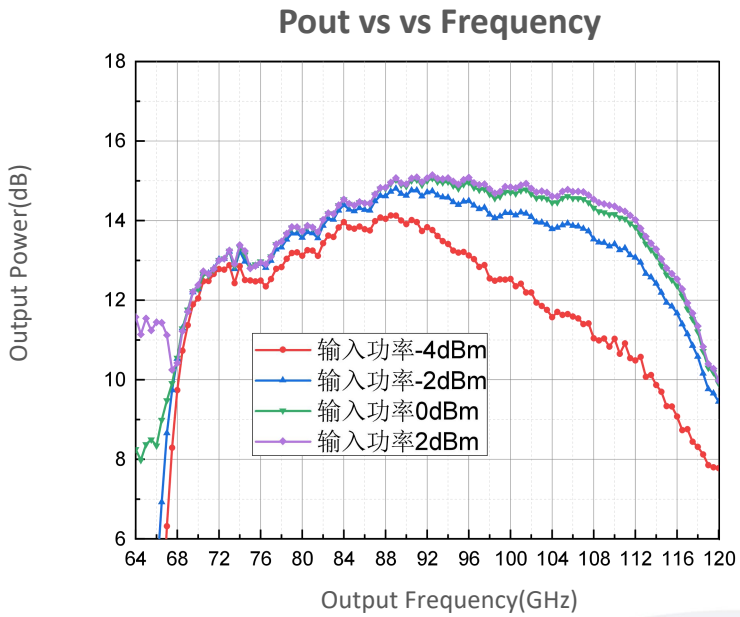
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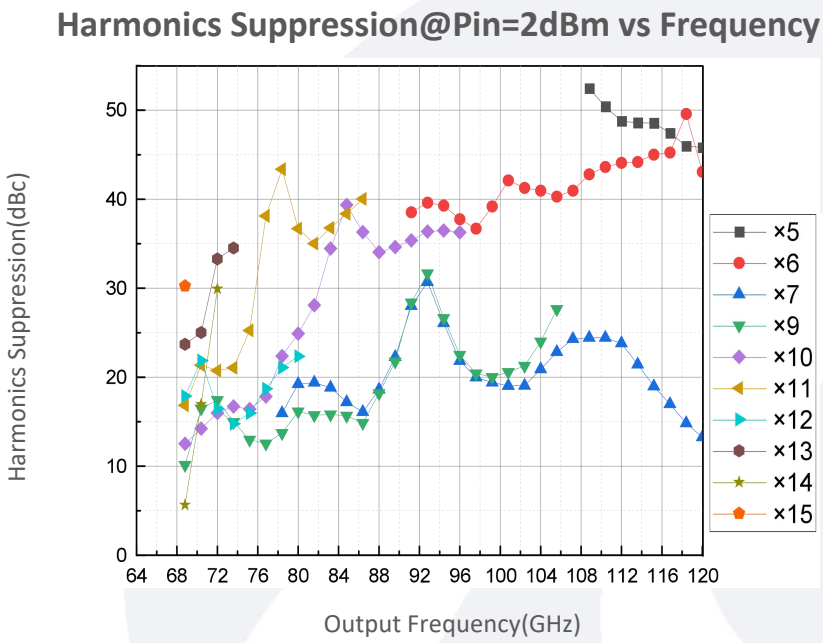
Definition of Bonding Point:

PAD	Symbol	Function	Dimension(μm²)
RFin Bonding Point			
1	GND	Ground	100x50
2	RFin	50 Ohm, open circuit for DC	50x50
3	GND	Ground	100x50
RFout Bonding Point			
4	GND	Ground	100x50
5	RFout	50 Ohm, open circuit for DC	50x50
6	GND	Ground	100x50
DC Bias Bonding Point			
7	VG1	0.6V	50x50
8	VD1	3.3V/12.3mA	50x50
9	VD2	3.3V/6.25mA	50x50
10	VG2	-0.6V	50x50
11	VG3	-0.15V	50x50
12	VD3	3.3V/77mA	50x50
13	VG4	-0.15V	50x50
14	VD4	3.3V/62.3mA	50x50
15	VD5	3.3V/62.3mA	50x50
16	VG5	-0.15V	50x50
17	VD6	3.3V/77mA	50x50
18	VG6	-0.15V	50x50
19	VD7	3.3V/2.84mA	50x50
20	VG7	-0.6V	50x50
21	VD8	3.3V/12.3mA	50x50
22	VG8	0.6V	50x50
23	VG9	-0.08V	50x50

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Typical Performance Data:

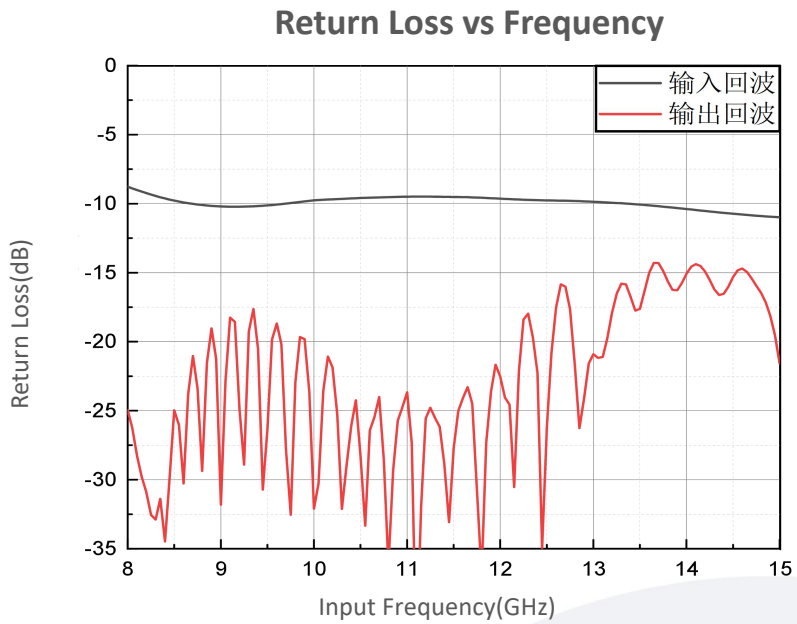




Note: Above data is for ref only, actual data may vary from unit to unit depending on operating environment and other factors like material lots etc.

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Simulation Data:



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Application Information:

1、 Storage: The chip must be placed in a container with electrostatic protection function and stored in nitrogen environment.
2、Cleaning: The bare chip must be operated and used in a purified environment. It is forbidden to use liquid detergent to clean the chip.
3、 Electrostatic protection: Please strictly comply with ESD protection requirements to avoid electrostatic damage.
4、 Routine operation: Please use vacuum chuck or precision pointed tweezers to take the chip. Avoid touching the chip surface with tools or fingers during operation.
5、 Power on sequence: when power on, apply gate voltage first and then Drain voltage; When de energizing, remove the Drain voltage first and then the gate voltage.
6、 Mounting operation: The chip can be installed by AuSn solder eutectic sintering or conductive adhesive bonding process. The installation surface must be clean and flat, and the gap between the chip and the input / output RF connecting line substrate shall be as small as possible.
Sintering process: 80 / 20 AuSn shall be used for sintering. The sintering temperature shall not exceed 300 ℃, the sintering time shall be as short as possible, not more than 20 seconds, and the friction time shall not exceed 3 seconds.
Bonding process: The dispensing amount of conductive adhesive shall be minimized during bonding, and the curing conditions shall refer to the data provided by the conductive adhesive manufacturer.
7、 Bonding operation:
Unless otherwise specified, two bonding wires (diameter 25um gold wire) are used for RF input and output, and the bonding wire shall be as short as possible.
The thermal ultrasonic bonding temperature is 150 ℃, and the ultrasonic energy is as small as possible. The pressure of spherical bonding cleaver is 40 ~ 50gf, and the pressure of wedge bonding cleaver is 18 ~ 22gf.
8、 If you have any questions, please contact the supplier.